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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/716,721	11/20/2000	Thomas Edward Horlander	RCA 89,324 / PU000125	9573

24498 7590 11/03/2005

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EXAMINER

HO, CHUONG T

ART UNIT PAPER NUMBER

2664

DATE MAILED: 11/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/716,721

Applicant(s)

HORLANDER ET AL.

Examiner

CHUONG T. HO

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 24 February 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1,3-6,8 and 9 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1,3-6,8 and 9 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date <u>8</u> . | 6) <input type="checkbox"/> Other: _____ |

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1. Amendment filed 02/24/04 have been entered and made of record.
2. Applicant's amendment filed 02/24/04 with respect to claims 1, 3-5, 6, 8-9 have been considered but are moot in view of the new ground(s) of rejection.
3. Claims 1, 3-5, 6, 8-9 are pending.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 1, 3-5, 6, 8-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Swenson et al. (U.S. Patent No. 5,926,120) in view of Dally et al. (U.S. Patent No. 6,269,435 B1).

Regarding to claim 1, see figure 3, Swenson et al. discloses all the following subject matters: a serial compressed bus interface; comprising:

- A serial-to-parallel converter (see col. 2, lines 18-22) having a single serial data input line adapted to receive time-division multiplexed (41) serial data from a plurality of data sources (PI (0) – PI (7)), and having a plurality of parallel output lines for providing thereon a packet of time-division multiplexed (41) serial data in parallel form to one of a plurality of devices associated with data applications (51-58) ;

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- Enable logic (39) coupled to each of plurality of devices (51-58) and adapted to provide at least one data valid signal that identifies each of a plurality of data consumers (51-58) for which the time-division multiplexed (41) serial data is valid (see figure 3, col. 3, lines 19-21).

However, Swenson et al. is silent to disclosing enable logic adapted to provide at least one data valid signal that identifies which of a plurality of devices are associated with a particular packet.

Dally et al. discloses, see figure 6, enable logic adapted to provide at least one data valid signal that identifies which of a plurality of devices (FIFO 39, 36) are associated with a particular packet. (see col. 7, lines 48-54, When the data valid signal 44 is asserted, the True FIFO 34 is enabled to store the data value present on the input stream 32 when the condition stream 42 indicates that the data value satisfies a given condition).

Both Swenson and Dally discloses bit select or data valid signal. Dally recognizes enable logic adapted to provide at least one data valid signal that identifies which of a plurality of devices (FIFO 39, 36) are associated with a particular packet. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the system of Swenson with the teaching of Dally to provide at least one data valid signal that identifies which of a plurality of devices are associated with a particular packet in order to reduce the pin count within a switching element through the use of a multiplexer.

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5. Regarding to claim 6, see figure 3, Swenson et al. discloses all the following subject matters: a serial compressed bus interface; comprising:

- Time-division multiplexing (41) the serial compressed data from the plurality of data source (PI (0) – PI (7)) to generate time-division multiplexed serial compressed data onto a single data line (see col. 3, lines 15-21);
- Converting (see col. 2, lines 18-22) the time-division multiplexed serial data to a packet of parallel data (see col. 1, lines 15-22), and output packet of parallel data for receipt by at least one of plurality of devices (51-58) associated with data applications (see col. 4, lines 19-24);
- A serial-to-parallel converter (see col. 2, lines 18-22) having a single serial data input line adapted to receive time-division multiplexed (41) serial data from a plurality of data sources (PI (0) – PI (7)), and having a plurality of parallel output lines for providing thereon a packet of time-division multiplexed (41) serial data in parallel form to one of a plurality of devices associated with data applications (51-58) ;
- Enable logic (39) coupled to each of plurality of devices (51-58) and adapted to provide at least one data valid signal that identifies each of a plurality of data consumers (51-58) for which the time-division multiplexed (41) serial data is valid (see figure 3, col. 3, lines 19-21).

However, Swenson et al. is silent to disclosing enable logic adapted to provide at least one data valid signal that identifies which of a plurality of devices are associated with a particular packet.

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Dally et al. discloses, see figure 6, enable logic adapted to provide at least one data valid signal that identifies which of a plurality of devices (FIFO 39, 36) are associated with a particular packet. (see col. 7, lines 48-54, When the data valid signal 44 is asserted, the True FIFO 34 is enabled to store the data value present on the input stream 32 when the condition stream 42 indicates that the data value satisfies a given condition).

Both Swenson and Dally discloses bit select or data valid signal. Dally recognizes enable logic adapted to provide at least one data valid signal that identifies which of a plurality of devices (FIFO 39, 36) are associated with a particular packet. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the system of Swenson with the teaching of Dally to provide at least one data valid signal that identifies which of a plurality of devices are associated with a particular packet in order to reduce the pin count within a switching element through the use of a multiplexer.

6. Regarding to claim 3, Swenson et al. discloses a request control circuit (selector 42) adapted to output at least one request signal that requests the time-division multiplexed (41) serial data for at least one of the plurality of devices (51-58) associated with data applications (see col. 4, lines 19-21).

7. Regarding to claim 4, Swenson et al. discloses at least one encoder (address 39) adapted to encode at least one of the at least one data valid signal and the at least one request signal to corresponding to more than one plurality of devices (51-58) with data applications (see col. 4, lines 18-21).

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8. Regarding to claim 5, Swenson et al. discloses the request control circuit (selector 42) is further adapted to encode the at least one request signal to correspond to more than one of the plurality of device (51-58) associated with data applications (see col. 4, lines 18-21).
9. Regarding to claim 8, Swenson et al. discloses the step of encoding a data valid signal (the bit select signal 43) to indicate the time-division multiplexed serial compressed data is valid for more than one of devices (51-58) associated with data application (see col. 5, lines 13-16, col. 4, lines 60-62).
10. Regarding to claim 9, Swenson et al. discloses the step of encoding a request signal (bit select signal 43) to indicate that the time-division multiplexed serial compressed data is requested by more than one devices associated with data applications (see col. 5, lines 13-16, col. 4, lines 60-62).

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

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the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to CHUONG T. HO whose telephone number is (571) 272-3133. The examiner can normally be reached on 8:00 am to 4:00 pm.

The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

10/28/05

A handwritten signature in black ink, appearing to be 'W. Chin', with a long horizontal line extending to the right.

WELLINGTON CHIN
ADVISORY PATENT EXAMINER